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ECe 3200-01 Lab 5

CE Amplifier with a Series Unbypassed Emitter Resistance (Mid-band Frequency Range)

**Objective:**

The objective of this lab is to design a CE amplifier to meet a specific bias condition and a specified voltage gain of . This will be accomplished by introducing a small un bypassed resistor in series with the emitter. The performance parameters, Av, Ri, and Ro will be measured and compared versus the calculated ones.

**Prelab:**

Diagram, schematic

Description automatically generated

1. Use a 2N3904 NPN transistor (or equivalent) and use a curve tracer to determine the ac and dc current gains and ro at the Q-point. (You may assume the current gain is about 100 and ro = ∞ or see the data sheets)
2. Calculate R1 and R2 by the method of setting IR1 = 10x IBq and IR2 = 9xIBq using standard resistors.
3. Calculate RC and RE for the bias point of ICq = 1.1 mA. VCEq = 5.3 V, VCC = 12 V, VE ≈ 20%VCC.
4. Determine a suitable value for rE , the emitter series resistance , so that the ac voltage gain Av ≈ 20 . Usually, this resistor is much smaller than RE and has very little influence on the dc condition, but it will strongly affect the ac voltage gain and Ri.
5. Draw the small signal equivalent circuit and validate the following equation statements for the voltage gain (Av), input impedance (Ri) and the output impedance (Ro):

Ri = R1 || R2 || [ rπ + (1 + β rE)] ……….. (1)

AV = vo / vi = -β\*RC /[ rπ + (1 + β)rE ] …….(2)

Ro ≈ Rc ……….(3) - Assuming VA = ∞ i.e ro the collector to emitter resistance is ∞)

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**Procedure:**

1. Assemble the circuit of fig 1 with your calculated values and measure the Q-points.

ICq = 1.13 mA , VCEq = 5.55V , VEq = 2.462V , VBq = 3.162V

Diagram, schematic

Description automatically generated

1. Set the signal generator output vg = 300 mVpp at 5 kHz. Make sure the output is a clean sinusoidal waveform free from distortion.
2. Measure the signals vi and vo.

vi = 145.086mV, vo = 2.66V

Graphical user interface

Description automatically generated

A screenshot of a computer

Description automatically generated with medium confidence

Compute the voltage gain, Av, from the measured signals Av = vo / vi

Av = 20 (Theoretical Value)

Av = 18.334 (Measured Value)

Av (% error) = 8.33%

**Compare** the result versus the value from equation (2). Discuss the difference.

1. Compute the input signal current, i in , from i in = ( vg – vi ) / Rg.

Then compute the small signal input impedance Ri with the measured signals,

Ri = vi / iin = 12.9 kΩ (Theoretical Value)

Ri = vi / iin = 12.81 kΩ (Measured Value)

Ri (% error) = 0.697674%

1. Now introduce the variable load resistor, RL, by connecting to the circuit. Note the output amplitude will drop. Continue decreasing RL till the output amplitude halves.

Remove RL and measure its resistance. The value is the equivalent to the output resistance at the output terminal (or equivalent to the Thevenin resistance viewed towards the circuit).

Diagram, schematic

Description automatically generated

RL = Ro = 3.6kΩ

A screenshot of a computer

Description automatically generated

**Compare** the result versus the value from equation (3). Discuss the difference.

RL = Ro = 3.9 kΩ (Theoretical Value)

RL = Ro = 3.6 kΩ (Measured Value)

RL (% error) = 7.69231%

1. With the measured values of Av, Ri and Ro draw a linear model with a voltage dependent source, an input impedance, and an output impedance, with vi as the independent input variable. Show it in your report.
2. Measure the power gain of the stage, Ap, when the load resistance is RL = 6 kΩ.

Ap = Po / Pi = (vo2 / RL) / (vi2 / Ri ) = (Ri / RL )( vo / vi )2 =

= (Ri / RL) Av2(Loaded)= 717.6 (4)

Where Pi is the input power, Po is the output power and Av (Loaded) is the voltage gain under the loaded condition.

1. Notice that also a small signal will be present at the emitter node ( ve ). The voltage gain (Ae) pertaining to the emitter port will be:

A e = ve / vi = ( 1 + β ) rE / [ rπ  + ( 1 + β ) rE ] …… (5)

The value of Ae is usually just under unity. Measure ve and vi and compute Ae. Compare with the equation (5).

Ae = 16.97

**Hint:**

Simplifying assumption is always helpful in an initial design. If you can make them use them for initial calculations. Specially regarding AV. Notice if (1+ β) rE >> rπ and β >>1 then β/ ( 1 + β ) ≈ 1 , then Av ≈ - Rc /rE. So as soon as RC is determined to satisfy the dc bias specifications then rE will follow.

**Conclusion:**

This lab was conducted to examine the differences in biasing of an NPN and PNP. As a result of this lab, I was able to better understand how to construct a basic CE amplifier to meet specific bias conditions and a specific voltage gain, Av. By utilizing the 2N3904 NPN transistor and pSpice, I was able to determine the AC and DC current gains as well as the output resistor value at the quiescent values. It was also very helpful being able to see where and how the input and output impedances are generated. Although I was not able perform the lab physically, I was still able to visualize and understand the circuit with the help of PSpice, and the zoom meeting provided. The lab was relatively similar to last week so it was easier to understand and perform correctly.